What is Claimed Is:

1. A method of manufacturing a semiconductor device, the method comprising:
forming an opening in a dielectric layer;
depositing a barrier layer lining the opening;
depositing a seed layer for copper (Cu) or Cu alloy deposition on the barrier layer;
depositing a conformal seed layer enhancement film by electroplating on the seed layer;
thermal annealing the seed layer enhancement film; and
filling the opening with Cu or Cu alloy.

2. The method according to claim 1, comprising depositing the seed layer by physical vapor deposition, wherein the deposited seed layer exhibits discontinuities.

3. The method according to claim 2, wherein the seed layer comprises Cu or Cu alloy.

4. The method according to claim 2, comprising depositing the seed layer at an equivalent surface deposition thickness of 300 Å to about 1,500 Å.

5. The method according to claim 2, comprising depositing the seed layer enhancement film as a conformal film bridging the discontinuities in the seed layer.

6. The method according to claim 5, comprising depositing the conformal seed layer enhancement film at a thickness of about 50 Å to about 300 Å.

7. The method according to claim 1, comprising thermal annealing by heating at a temperature of about 100°C to about 250°C.

8. The method according to claim 7, comprising thermal annealing in an inert or reducing atmosphere.

9. The method according to claim 8, comprising thermal annealing in an atmosphere comprising nitrogen, argon or a forming gas mixture containing hydrogen and nitrogen.

10. The method according to claim 9, comprising thermal annealing for about 1 minute to about 30 minutes.

11. The method according to claim 1, comprising depositing a composite barrier layer comprising a layer tantalum nitride lining the opening and a layer of α-tantalum on the tantalum nitride layer.

12. The method according to claim 13, comprising depositing the composite barrier layer at a combined equivalent surface deposition thickness of 100 Å to 400 Å.

13. The method according to claim 1, wherein the opening comprises a dual damascene opening having a lower via hole section in communication with an upper trench section, the method comprising filling the opening with Cu or Cu alloy to form a lower via in communication with an upper line.

14. The method according to claim 13, wherein the dual damascene opening is formed dielectric material having a dielectric constant no greater than about 3.9.

15. The method according to claim 14, wherein the dual damascene opening is formed in dielectric material comprising a fluorine (F) -containing oxide.

16. The method according to claim 5, wherein the deposited seed layer enhancement film exhibits a rough surface, the method comprising thermal annealing to reduce the roughness of the seed layer enhancement film.

17. The method according to claim 16, wherein the deposited seed layer enhancement film exhibits an average surface roughness (Ra) up to 40 Å, the method comprising thermal annealing to reduce the Ra of the seed layer enhancement film to about 19 Å to about 25 Å.

18. The method according to claim 16, wherein the deposited seed layer enhancement film exhibits a resistivity of about 2.5 to about 6 microOhm-cm, the method comprising thermal annealing to reduce the resistivity of the seed layer enhancement film to about 2.0 to about 3 microOhm-cm.